



General Certificate of Education (A-level)
June 2011

Electronics

ELEC1

(Specification 2430)

Unit 1: Introductory Electronics

Final

Mark Scheme

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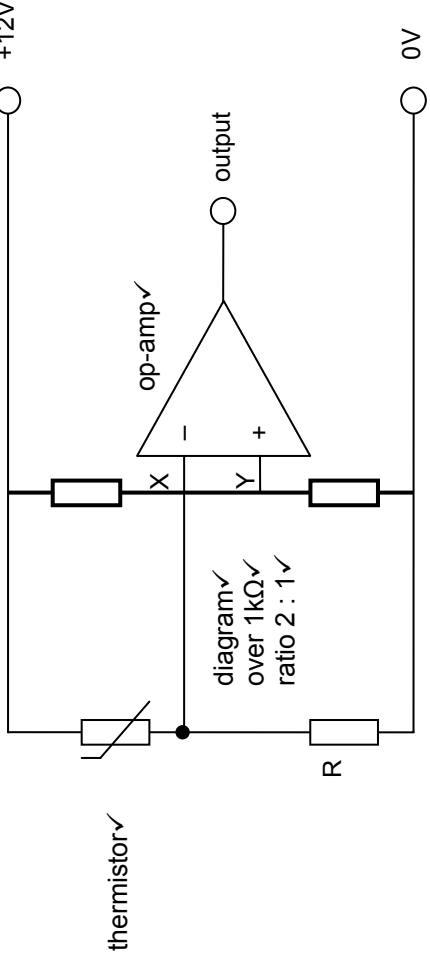
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Question	Part	Subpart	Marking guidance			Mark
1	(a)		humidity sensor ✓ comparator ✓ latch ✓ astable ✓ driver ✓ awd ✓ reset switch ✓ set level ✓			8
1	(b)	(i)	Set level✓			1
1	(b)	(ii)	Comparator✓			1
1	(b)	(iii)	Driver✓			1
2	(a)		$D = A.C✓$ $E = A.B✓$ $F = B.C✓$			3
2	(b)		$G = A.C + A.B✓$ $Q = A.C + A.B + B.C✓$			2

2	(c)			5
2	(d)	Output is a logic 1 when at least 2 inputs are at logic 1✓		1
3	(a)	(i) zener diode✓		1
3	(a)	(ii) 4.7V✓		1
3	(a)	(iii) reverse✓		1
3	(b)	(i) $5 + 100 = 105\text{mA}$ ✓		1
3	(b)	(ii) $10 - 4.7 = 5.3\text{V}$ ✓		1
3	(b)	(iii) $5.3 \div 0.105 = 50.5\Omega$ ✓		2
3	(b)	(iv) 47Ω ✓		1
3	(c)	(i) $14.4 - 4.7 = 9.7\text{V}$ ✓ $9.7 \div 33 = 294\text{mA}$ ✓		2
3	(c)	(ii) $4.7 \times 0.294 = 1.38\text{W}$ ✓		1

4	(a) & (b)				5
4	(c)	thermistor 20kΩ at 20°C ✓ 2 : 1 ratio (or calc) ✓ R = 10kΩ ✓			3
4	(d)	(i)	0V ✓		1
4	(d)	(ii)	>0 – 3V ✓		1
5	(a)	base ✓	gate ✓		2
5	(b)	MOSFET ✓			1
5	(c)	needed to limit the current to a safe value ✓	in the base ✓		2
5	(d)	(i)	protection diode – correct symbol and position ✓ correct way round ✓		2

5	(d)	(ii)	protection diode/back emf diode ✓ to prevent damage to transistor/prevent back emf when MOSFET switches off ✓		2
5	(e)		MOSFET has high input resistance ✓ so less current needed from input ✓ because logic circuit can't provide enough current for NPN transistor ✓ larger current gain needed for motor switch than for light switch ✓ (max 3)		3
6	(a)		Logic 1 on top line only, all rest are zeroes. ✓		1
6	(b)		One term per line that gives $P=1$ ✓ 7 terms in all ✓ Each term has all four variables, ✓ with bars where values are zero All "OR"ed together ✓ (✓✓ max)		2

6	(c)	The Boolean Algebra solution is obtained by adding redundant terms into the expression for P; term 3 is repeated three times and term 4 twice. Dbar.A is then obtained by factorising terms 1,3,4 and 5, which contain all possible combinations of variable B and C which can therefore be removed. Cbar.B.A is obtained by factorising terms 3 and 6, variable D is removed as D + Dbar is equivalent to logic 1, which anded with the remaining variables, goes out. C.Bbar.A is obtained from terms 4 and 7, variable D is removed as D + Dbar is equivalent to logic 1, which anded with the remaining variables, goes out. Dbar.Cbar.B is obtained from terms 2 and 3, variable A is removed as A + Abar is equivalent to logic 1, which anded with the remaining variables, goes out.			4
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6	(d)			
5				

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